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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,231	02/19/2004	Lothar Benedict Erhard Josef Moeller	Moeller 19-8	5230

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EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
2613	

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06/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,231	MOELLER ET AL.	
	Examiner	Art Unit	
	David S. Kim	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,11,13-20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,11,13-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 02 April 2007. These drawings are approved.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as Josef Moeller (U.S. Patent Application Publication No. US 2003/0170022 A1, hereinafter "Moeller") at the time this invention was made, or was subject to a joint research agreement at the time this invention was made. However, reference Moeller additionally qualifies as prior art under another subsection of 35 U.S.C. 102, and therefore, is not disqualified as prior art under 35 U.S.C. 103(c).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the invention of this application, and is therefore, not the invention "by another," or by antedating the applied art under 37 CFR 1.131.

5. **Claims 1, 3, 5, 7-9, 11, 14-20, and 22-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moeller.

Regarding claim 1, Moeller discloses:

A method of signal processing, comprising:

converting an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal (e.g., 230 in Fig. 2, 530 in Fig. 5);

sampling the electrical signal using two or more sampling windows contained within a time interval having a one-bit length (the multiple sampling points in Fig. 4 correspond to one bit slot) to generate two or more bit estimate values (multiple sampling points in Fig. 4), wherein sampling the electrical signal comprises:

integrating the electrical signal over a first sampling window to generate a first integration result (integration for the left sampling point in Fig. 4 is implied in the decision circuit 240 to generate the output bit estimate values);

comparing the first integration result with a first decision threshold value to generate a first bit estimate value (e.g., threshold in Fig. 4);

integrating the electrical signal over a second sampling window to generate a second integration result (integration for the right sampling point in Fig. 4 is implied in the decision circuit 240 to generate the output bit estimate values); and

comparing the second integration result with a second decision threshold value to generate a second bit estimate value (e.g., threshold in Fig. 4); and

applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5).

Moeller does not expressly disclose:

wherein applying the logical function comprises applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) logic circuitry. Still, Moeller does disclose the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is a "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability for a particular bit estimate value, e.g., "0" values.

Regarding claim 3, Moeller discloses:

The method of claim 1, wherein:

each sampling window has a width (each sampling point in Fig. 4 has its own finite width);

the electrical signal has a series of waveforms comprising first and second pluralities of waveforms, wherein each waveform of the first plurality represents a binary "0" and each waveform of the second plurality represents a binary "1" (waveforms below the threshold represent "0", waveforms above the threshold represent "1"); and

for each sampling window:

a waveform is integrated over the sampling window width to generate a corresponding bit estimate value (integration is implied in the decision circuit 240 to generate the output bit estimate values); and

Moeller does not expressly disclose:

the sampling window width is selected to reduce contribution of the second plurality of waveforms into integration results corresponding to the first plurality of waveforms.

However, such a selection of sampling window width is intuitively obvious. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to provide such a

selection of sampling window width. One of ordinary skill in the art would have been motivated to do this in view of an obviously undesirable counterexample. That is, consider the option of a sampling window that is as wide as the bit slot. With such a wide sampling window, the "1" waveforms of pulses with timing jitter from adjacent bit slots can adversely contribute to the integration results corresponding to "0" waveforms. This contribution can lead to inaccurate sampling results. Accordingly, it follows that one would be motivated to select a sampling window width to reduce this contribution, e.g., a sampling window width that is narrower than the bit slot.

Regarding claim 5, Moeller does not expressly disclose:

The method of claim 1, wherein the first decision threshold value is different from the second decision threshold value.

However, setting different threshold values is an obvious practice for the method of Moeller. One of ordinary skill in the art would have been motivated to do this to provide design flexibility in addressing various sources of noise in decision circuit 240, with consideration of timing jitter. For example, lower threshold values may help avoid spontaneous beat noise at the mark level of a sampling window, and higher threshold values may help avoid spontaneous beat noise and thermal noise at the space level of a sampling window. Employing different threshold values at different sampling points allows one to vary the influence of these various sources of noises at different sampling points, thus providing a practitioner with the ability to tailor the operation of decision circuit 240 for various bit patterns.

Regarding claim 7, Moeller discloses:

The method of claim 1, comprising:

generating a first clock signal based on the electrical signal (10 GHz clock tone in paragraph [0021]);

multiplying a frequency of the first clock signal to generate a second clock signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]); and

sampling the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values (sampling according to the 40 GHz clock in paragraph [0021]).

Regarding claim 8, Moeller discloses:

The method of claim 7, comprising:

separating the first and second bit estimate values from the bit stream while discarding all other bits of the bit stream (demultiplexer 250 in Fig. 2).

Regarding claim 9, Moeller discloses:

The method of claim 1, comprising:

generating a clock signal based on the electrical signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]);

sampling first and second copies of the electrical signal at a sampling rate corresponding to the clock signal (sampling according to the 40 GHz clock in paragraph [0021]), wherein:

the first copy is sampled to generate the first bit estimate value (values of top input to gate 260 in Fig. 2);

the second copy is sampled to generate the second bit estimate value (values of bottom input to gate 260 in Fig. 2); and

the first and second copies are sampled with a relative time delay (delay 280 in Fig. 2).

Regarding claim 11, Moeller discloses:

An optical receiver, comprising:

a signal converter adapted to convert an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal (e.g., 230 in Fig. 2, 530 in Fig. 5); and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length (the multiple sampling points in Fig. 4 correspond to one bit slot) to generate two or more bit estimate values (multiple sampling points in Fig. 4);

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5);

(iii) integrate the electrical signal over a first sampling window to generate a first integration result (integration for the left sampling point in Fig. 4 is implied in the decision circuit 240 to generate the output bit estimate values);

(iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value (e.g., threshold in Fig. 4);

(v) integrate the electrical signal over a second sampling window to generate a second integration result (integration for the right sampling point in Fig. 4 is implied in the decision circuit 240 to generate the output bit estimate values); and

(vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value (e.g., threshold in Fig. 4).

Moeller does not expressly disclose:

wherein the decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) logic circuitry. Still, Moeller does disclose the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is a "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the apparatus of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability for a particular bit estimate value, e.g., "0" values.

Regarding claim 14, Moeller discloses:

The receiver of claim 11, comprising:

a decision circuit (e.g., decision circuit 240 in Fig. 2) coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal (implied circuitry for recovering the 10 GHz clock tone in paragraph [0021]); and

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]), wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying first and second bit estimate values (sampling according to the 40 GHz clock in paragraph [0021]).

Regarding claim 15, Moeller discloses:

The receiver of claim 14, comprising:

a de-multiplexer (250 in Fig. 2) having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit (240 in Fig. 2);

a first output port is adapted to receive a signal corresponding to the first bit estimate value (top output port to gate 260); and

a second output port is adapted to receive a signal corresponding to the second bit estimate value (bottom output port to gate 260), wherein the "AND" gate is coupled to the first and second output ports (see the treatment of claim 11 above regarding this "AND" gate limitation).

Regarding claim 16, Moeller discloses:

The receiver of claim 11, comprising:

first and second decision circuits (560_1 and 560_2 in Fig. 5), each coupled to the signal converter;

a clock recovery circuit (10 Gb/s Clk) coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal (sampling in paragraph [0034]);

the first decision circuit is adapted to generate the first bit estimate value (e.g., 560_1 in Fig. 5);

the second decision circuit is adapted to generate the second bit estimate value (e.g., 560_2 in Fig. 5); and

the first and second decision circuits sample the electrical signal with a relative time delay (time delay in Fig. 5).

Regarding claim 17, Moeller does not expressly disclose:

The receiver of claim 16, wherein the "AND" gate is coupled to the first and second decision circuits (see the treatment of claim 11 above regarding this "AND" gate limitation).

Regarding claim 18, Moeller discloses:

The receiver of claim 16, wherein each decision circuit is adapted to:

integrate the electrical signal over a respective sampling window to generate a respective integration result; and

compare the respective integration result with a respective decision threshold value to generate a bit estimate value (integration is implied in the decision circuit 240 to generate a respective integration result for comparison with a respective decision threshold of Fig. 4 to generate the output bit estimate values).

Regarding claim 19, Moeller does not expressly disclose:

The receiver of claim 18, wherein the first and second decision circuits use different decision threshold values.

Claim 5 introduces a similar limitation. An obviousness argument is applied to address this similar limitation in the treatment of claim 5 above. Similarly, the same obviousness argument is applied here to address this corresponding limitation in claim 19.

Regarding claims 20 and 22-25, claims 20, 22, 23, 24, and 25 are system claims that introduce limitations that correspond to the limitations introduced by receiver claims 11, 13, 15, 17, and 19, respectively. Therefore, the recited means in receiver claims 11, 13, 15, 17, and 19 read on the corresponding means in system claims 20 and 22-25.

6. **Claims 6 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moeller as applied to the claims above, and further in view of Yonenaga et al. ("Dispersion-tolerant optical transmission system using duobinary transmitter and binary receiver", hereinafter "Yonenaga").

Regarding claim 6, Moeller does not expressly disclose:

The method of claim 1, wherein the optical signal is an optical duobinary signal.

Although Moeller considers return-to-zero (RZ) coding (paragraph [0017]), notice the duobinary coding of Yonenaga (p. 1530, col. 2, middle paragraph – p. 1531, 1st paragraph). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to employ the duobinary coding of Yonenaga. One of ordinary skill in the art would have been motivated to do this for any of the following advantages: higher tolerance to fiber chromatic dispersion that limits transmission distance and suppression of stimulated Brillouin scattering (SBS) (Yonenaga, p. 1530-1531, bridging paragraph).

Regarding claim 13, Moeller in view of Yonenaga discloses:

The receiver of claim 11, wherein the optical signal is an optical duobinary signal (Yonenaga, p. 1530, col. 2, middle paragraph – p. 1531, 1st paragraph).

Response to Arguments

7. Applicant's arguments filed on 02 April 2007 have been fully considered but they are not persuasive. Applicant argues that Moeller is excluded under 35 USC 103(c) (REMARKS/ARGUMENTS, p. 7, 4th paragraph). However, reference Moeller additionally qualifies as prior art under another subsection of 35 U.S.C. 102, and therefore, is not disqualified as prior art under 35 U.S.C. 103(c). Therefore, Applicant's arguments are not persuasive. Accordingly, Examiner respectfully maintains the standing rejections.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

Approved by DSK
02 JUNE 2007

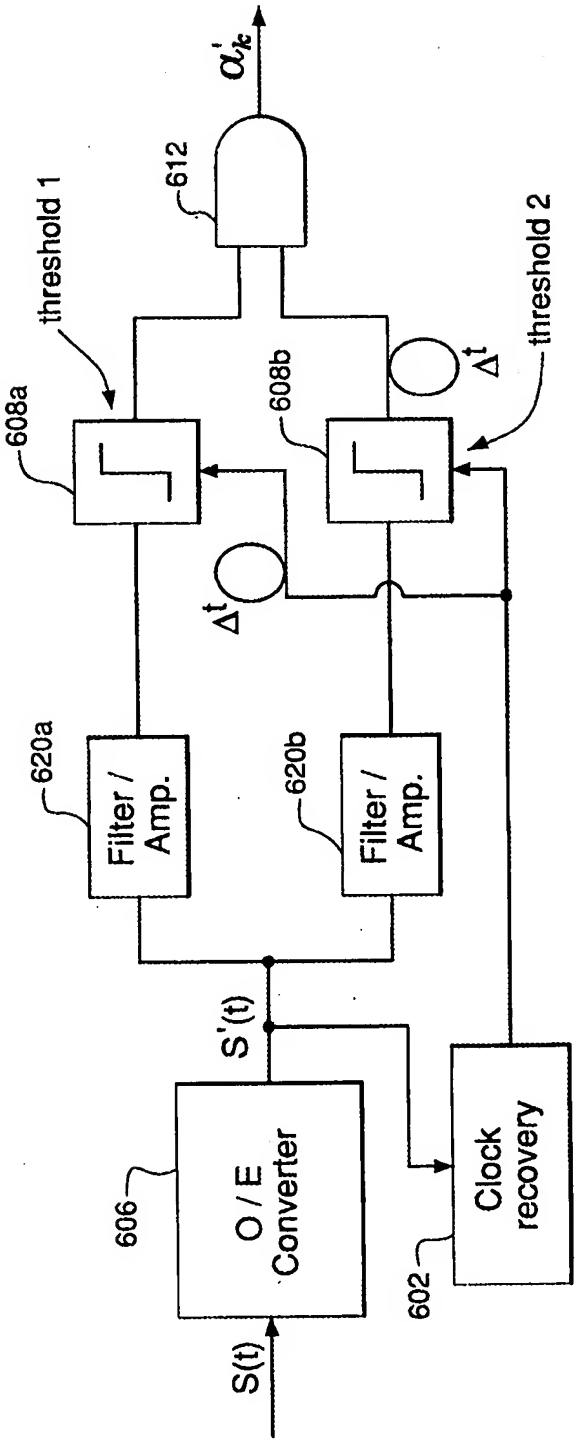

FIG. 6

Annotated Marked-up Drawing

Approved by DSK
02 JUNE 2009

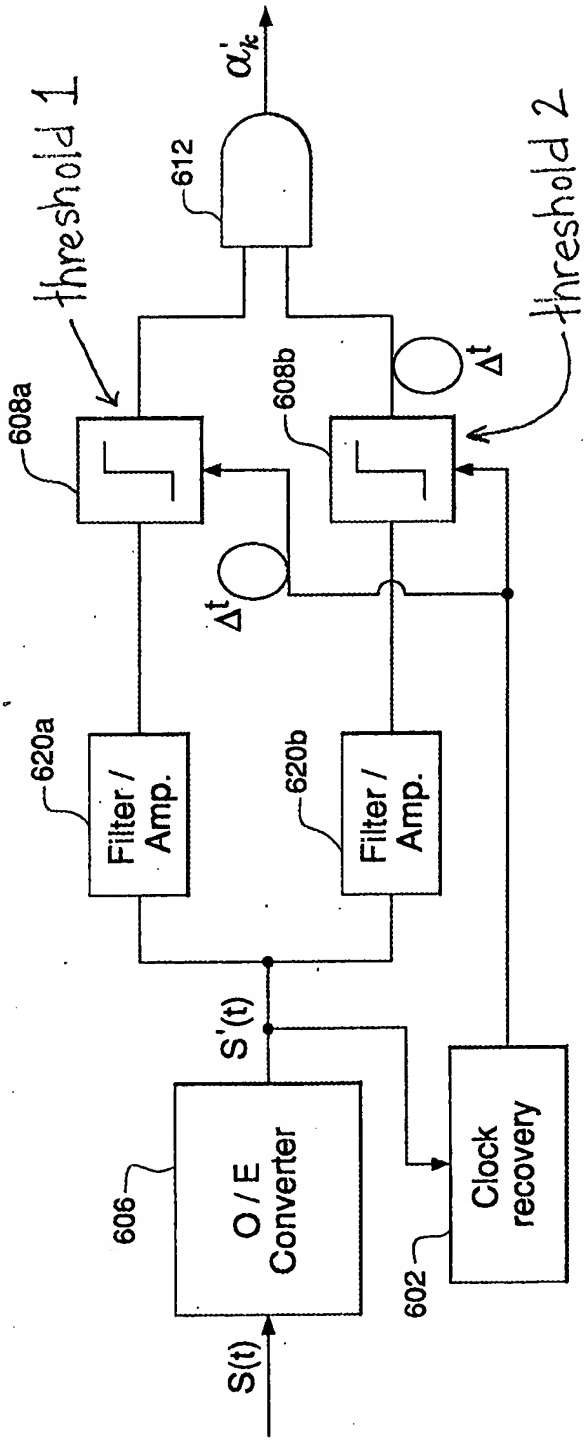

FIG. 6